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Built-In self test : test solution for telecommunication systems

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ABSTRACT : The technological revolution witnessed by the telecommunications industry is leading to the development of new applications, products and protocols, which in turn solicits widely accessible, highly reliable and high quality networks. To meet the stringent quality and reliability requirements of today's complex communication networks, efficient test methodologies are necessary at all levels. Conventional test methodologies are being constantly challenged by ever-increasing speed and size, which results in high costs associated with test hardware, test generation and test application time. To meet the high quality and reliability requirements for complex communication networks, efficient test methodologies are employed at all levels – system/equipment, board, integrated circuits and so on. Built-in self test (BIST) offers a test methodology where the test functions are embedded into the circuit itself. The advantage of using BIST for complex telecommunication systems are : reduced test development time, low test application time, provision for at-speed tests, in-field test capability and high fault coverage.

This paper explores the Built-in Self Test concept to test a telecommunication system off-line as well as on-line. The proposed design methodology is to detect and probably diagnose faults in networked equipments by incorporating Network Management System.

Keywords : Telecommunication, Network Management System, Built-in Self Test, Automatic Test Equipment, Pseudo-random Sequence, Faults, Tests, Verification etc

I. INTRODUCTION

The telecommunication industry is witnessing a rapid technological revolution : wired networks are giving way to wireless networks and application, data networks are expanding at an exponential rate, and the availability of bandwidth is resulting in more and more information being packed and transmitted simultaneously. These factors are leading to the development of new applications, products and protocols, resulting in better methods for establishing a widely accessible, high-quality and reliable network. Furthermore, present networks comprise different types of equipment requiring efficient integration thereby accentuating easy flow of information. To meet the high quality and reliability requirements for complex communication networks, efficient test methodologies are employed at all levels-system, board, integrated circuits and so on.

This can be achieved by incorporating built-in test capabilities that monitor the system functionality periodically in the field against any failures, as well as reliable hardware components that are thoroughly tested for structural defects. To guarantee the highest level of reliability for telecommunication devices, in addition to offline test, continuous online monitoring of system functionality for transient failures and efficient support for fault recovery and management are necessary. This can be achieved by implementing concurrent fault detection and diagnosis.

Service providers today face many challenges. Network topologies are growing more complex, new technologies for service delivery must be integrated into their networks, and customers are more demanding and fickle than ever before. One of the most important requirements for assuring the timely delivery of services without interruption is a network management system that is flexible enough to provide visibility within a complex network. Today's network management systems require improved price/performance, high density, low power consumption, field programmability, modularity for scalability, and carrier-grade availability [1].

The network manager must offer fast time-to-revenue with efficient service provisioning, fast response to network changes and quick troubleshooting capabilities. The remote configuration, automated processes and templates reduce the need for site visits and the time to deliver services. Thanks to advanced testing tools, it is now possible to test the network before deploying services in a live network. The manager is expected to provide accurate and on-time data for service-level reporting purposes. The manager must be designed for carrier-class performance from day one. In practice this means a highly reliable platform that can grow in a controlled way as the network grows.

II. TELECOMMUNICATION NETWORK

PDH or the plesiochronous digital hierarchy is a popular technology that is widely used in the networks of telecommunication in order to transport the huge amount of

data over the digital equipment for transportation like microwave radio or fiber optic systems.

PDH network equipment *i.e.*, Optical Line Terminal Equipment (OLTE) is now quite physically small, allowing for its deployment in locations other than a telephone exchange. PDH Networks are ideal choice for low traffic networks belonging to sectors other then Telecommunication companies like Oil & Gas, Railways, process plants, other manufacturing units where stations are almost unmanned and topology is point to point with bus, star, ring architecture etc.

PDH systems are generally used only for point-to-point communications systems because the signals must be fully multiplexed and then demultiplexed to access a single information channel. In addition, proprietary alarm configuration and management means that equipment at either end of a PDH system must be from the same manufacturer. Moreover PDH systems are manufacturer-specific systems. Non availability of world standard on the digital formats, asynchronous structure that is rigid, multiplexer mountains, no integrated network management, restricted management capacity, no world standard optical interfaces makes networking almost impossible.

SDH systems have upper hand on PDH system. Some of the most common advantages enjoyed by the usage of SDH include: well defined optical interfaces, capability of powerful management, world standard digital format, synchronous structure is flexible, cost effective and easy traffic cross connection capacity and add and drop facility, reduced networking cost due to the transversal compatibility, forward and backward compatibility. But the SDH systems are available in high bit rates of 155 Mbps, 622 Mbps, 2.5 Gbps and 10 Gbps.

PDH Technology had been in play since 1980 and most of old systems/networks still operate on PDH. The traditional PDH network has long been tailored to the services generally provided i.e. voice, leased lines, and low rate data sometimes each by separate equipment and networks. With the advent of digital technology, the process of installation, maintenance have become less cumbersome and quality of services has improved. It is therefore felt that the any cause for dissatisfaction, among customers about present services, is predominantly due to the frequent failures in the network and the time taken for restoring them.

In PDH telecommunication systems, different and synergistic approaches have to be exploited to guarantee the required levels of performance, robustness, availability, and reliability. This paper explains how a 2 Mbps PDH Optical System can be modified to incorporate Network Management System (NMS) with Built-in Self Test facility. Proposed Network Management facility will provide various management capabilities such as performance management by detecting errors in the received optical signal, security by incorporating coding at transmitter end, access management by declaring one of the stations in the network as master, configuration management by operating the Optical Systems as Optical Line Terminal Equipment of Optical Regenerator with add-drop facility and the event or the alarm management for individual system.

The proposed modifications in the OLTE circuits are proposed to be implemented using complex and powerful very large scale integrated (VLSI) circuits that form the basic building blocks. This translates into increased component density and reduced feature sizes for application-specific IC, which, along with the complexity of modern designs, demand efficient test and verification techniques to guarantee good quality and reliable products. Conventional methods for manufacturing test of digital circuits are constantly challenged by ever-increasing speed and circuit size which solicit sophisticated automatic test equipment (ATE). This result in very high costs associated with test hardware, test generation and test application time. Furthermore, at-speed testing *i.e*., verification of system functionality rated speed, requires high-performance ATE, which results in a manifold increase in their price. Thus it proposed to equip the OLTE with Built-In Self-Test.

III. BUILT-IN SELF TEST

Built-In Self-Test (BIST) provides a feasible solution to the above demands. Built-in self test offers a test methodology where the test functions are embedded into the circuit itself. The test functions in BIST are localized to the circuit, thereby facilitating at-speed test and substantial reduction in test application time. Furthermore, BIST provides easy access to the embedded components and interconnections at the system level without any special test requirements [2].

BIST significantly reduces off-chip communication to overcome the bottleneck caused by the limited input/output access. Further, it eliminates much of the test pattern generation and simulation process. Testing time can be shorten by testing multiple units simultaneously through test scheduling. Hardware overhead can be minimized by careful design and through the sharing of test hardware [3].

For system architects, built-in self-test is nothing new. It describes the capability embedded in many high-availability systems, such as telephone switching systems, to execute thorough self-testing to detect the presence of hardware faults, and, if present, to isolate any fault to a replaceable unit. In this context, BIST complements other built-in system capabilities, such as parity checkers and watchdog timers, which run concurrently with system operation to detect abnormal conditions.

BIST is a design-for-testability technique that places the testing functions physically with the Circuit Under Test

(CUT), as illustrated in Fig.1. In normal operating mode, the CUT receives its inputs from other modules and performs the function for which it was designed. In test mode, a test pattern generator circuit Test Pattern Generator (TPG) applies a sequence of test patterns to the CUT, and the test responses are evaluated by a Output Response Analyzer (ORA). In the most com-mon type of BIST, test responses are compacted in ORA to form (fault) signatures. The response signatures are compared with reference signatures generated or stored on-chip, and the error signal indicates any discrepancies detected [4].

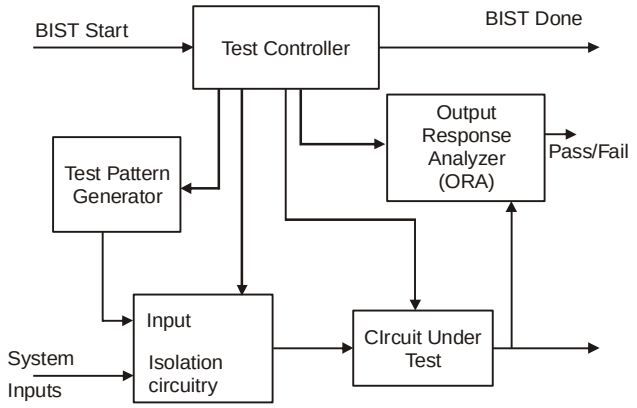

Fig.1. Architecture of built-in self test.

IV. TRADITIONAL OPTICAL COMMUNICATION SYSTEM

Traditional Optical Communication Systems consists of three major blocks of Transmitter, Receiver, Alarm Interface and optional Engineering Orderwire (EOW). Various alarms reported by the system are non-availability of signals electrical input and output signals, optical input and output signals, excessive current of laser diode, laser diode forcefully on, error major and error minors. Fig.2 gives the functional block diagram of traditional OLTE.

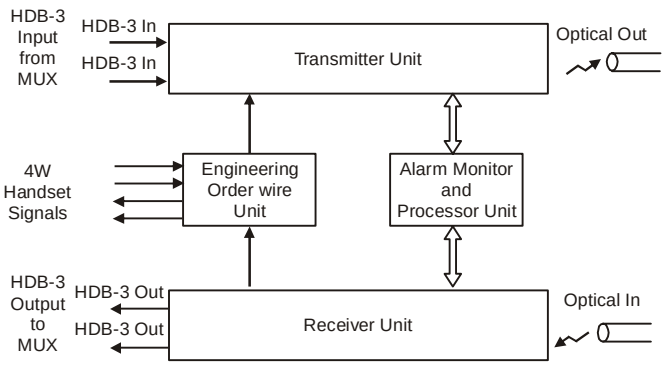

Fig.2. Functional block diagram of traditional optical line terminal equipment (OLTE).

V. PROPOSED OPTICAL COMMUNICATION SYSTEM

As compared to traditional Optical Communication Systems and proposed OLTE will consist of four major blocks of Transmitter, Receiver, Alarm Monitor and Processor, Multiplexer-Demultiplexer and optional Engineering Orderwire. Various alarms reported by the system are non-availability of signals electrical input and output signals, optical input and output signals, excessive current of laser diode, laser diode forcefully on, Automatic Gain Control, Unit not connected, all alarm signal indication, frame synchronisation loss, major fault in the system, error major and error minors. Apart from alarm reporting, values of certain parameters can also be observed, *e.g.*, various power supply, which unit is not connected, laser diode current, automatic gain control, error rate, clock failures. Fig.3 gives the functional block diagram of proposed OLTE.

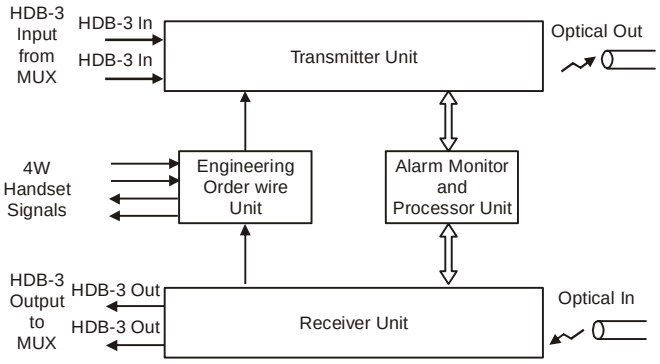

Fig.3. Proposed optical line terminal equipment.

It can be observed that a block of Multiplexer Demultiplexer has been added for transmission of alarm and monitoring signals from one station to another station. Multiplexer unit will be transmitting a frame with frame synchronization word. This word will be detected at receiver and than exchange of signals can take place between two or more stations. The current design supports 16 stations with reporting of 16 alarms and monitoring of 16 parameters. Sufficient space has been provided for future expansion. For security of data a encoder nBmB is also proposed. All these features will be implemented on a FPGA as blocks proposed and shown in Fig.4.

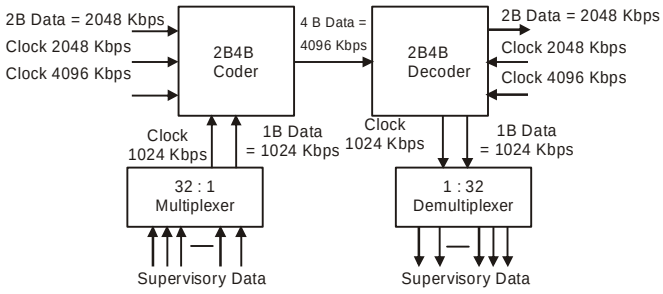

Fig.4. Functional block diagram for FPGA implementation.

VI. STRUCTURE OF SUPERVISORY FRAME OF MULTIPLEXER DEMULTIPLEXER UNIT

Position of bits	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Name of the bits	F1	F2	F3	EOWS	EOW	M1	M2	M3	M4	S1	S2	S3	S4	I1	R1	R2

Position of bits	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Name of the bits	R3	R4	R5	R6	EOW	C1	C2	A1	D1	D2	D3	D4	D5	D6	D7	D8

Fig.5. Structure of supervisory frame of multiplexer demultiplexer unit.

S.No.	**Name of the field**			**Remarks**
1.	F1-F3	:	Frame alignment word	Required for frame synchronization at remote station
2.	EOWS	:	Orderwire signalling fit	Required for call processing.
3.	EOW	:	Ordwewire fit	Required for carrying EOW data.
4.	M1-M4	:	Master address code	Indicates master station of the link *i.e.*, requesting station. At the most there can be 15 stations in the link.
5.	S1-S4	:	Slave address dode	Indicates the station address which is requested for information.
6.	I1	:	Call for information	Indicates certain information is required by the master.
7.	A1	:	Acknowledgement of call	The slave station acknowledges the call for request.
8.	D1 – D8	:	Data bits	Slave station sends in the information data via these 8-bits.
9.	R1 – R6	:	Requested information	Indicates type of information requested.
10.	C1 – C2	:	Configuration of the system	In all four configurations are OLTE, OREG and bypass.

Fig.6. Details of supervisory frame.

Fig.6 explains the meaning of each and every field of the Supervisory frame. Initially all fields except F1-F3, EOWS and EOW are transmitted as all ones. This frame is encoded and sent to receiver. At the receiver side the frame is recognised by matching frame alignment word. Once the frame alignment word is found, an indication to the transmitting station is send as an acknowledgement. The multiplexer now forms the NMS supervisory frame by multiplexing all the fields. This frame along with a mBnB coder incorporates the security features in the OLTE. The demultiplexer than demultiplexes the supervisory frame and sents the information of each and every bit to a central control unit for further processing [5].

The multiplexer-demultiplexer and nBmB coder-decoder will be implemented in a FPGA. This FPGA will incorporate BIST facility. The basic approach will be BIST insertion in the design during the test mode in such a ways that every logic block has a pseudo-random test pattern generator (PRPG) register at each of its inputs and MISR at its output. This can be done, if the registers are implemented as built-in logic block observers (BILBOs) that can be configured as either a PRPG or as an MISR [6].

Support for periodic in-field testing and diagnostics is another key requirement of highly reliable telecommunication devices. Traditional on-line testing is mostly based on space or time or information redundancy, wherein functional data is used as test input and replicated hardware and checkers are used for testing. Consequently, BIST structures used for offline production testing are different from the hardware structures used for in-field online testing. Deploying dedicated logic for offline BIST and online testing on the same VLSIC entails as much as 50% area overhead. Consequently alternate approaches during high-level design have been developed to investigate offline and online self-test by using offline BIST circuitry for online testing [7]. Unlike traditional online self-test approaches, these online BIST approaches do not use functional data as test input. Rather these online BIST approaches generate test patterns and compact test responses during the normal mode of operation. Furthermore, generation and application of test patterns and compaction of test responses are coordinated with the usages profile of the modules in the design. The key benefit of online BIST is that it is possible to run BIST in parallel with the functional chip and system test during production testing. This yields reduced test time. Furthermore faults are detected during field operation without taking the system offline. Also diagnostic information becomes continuously available. Finally the area overhead is less than the area overhead for dedicated offline BIST and online testing schemes [8].

VII. CONCLUSION

In this paper the implementation of Network Management System alongwith Built-in System Test for telecommunication systems is explained. Reduced test development time, low test application time, eliminating the need for very high-speed hardware testers, provision for at speed test, in-field test capability and high fault coverage are some of them. These factors easily out-weigh the disadvantages associated with BIST, such as area and performance overheads. The emerging system-on-a-chip design paradigm solicits good test solutions that will result in easy test integration and portability. BIST requires little effort to provide efficient test integration and hence is a sound alternative for nest generation designs.

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